20.8 A Fully Integrated Auto-Calibrated Super-Regenerative Receiver

Jia-Yi Chen, Michael P. Flynn, John P. Hayes

University of Michigan, Ann Arbor, MI

Applications such as sensor networks, implantable neuroprosthetic devices, robotics, and home automation, demand low-power and short-range wireless communication. A super-regenerative receiver has been demonstrated to provide low power consumption and small circuit area using an off-chip resonant tank and an externally controlled quench bias [1, 2]. The design in [3] incorporates an on-chip LC tank, but requires off-chip control to maximize sensitivity and selectivity. In this paper, a fully integrated super-regenerative receiver is presented that uses an auto-calibration scheme to eliminate off-chip control. The prototype receiver operates in the 2.4GHz ISM band with energy per received bit of 5.6nJ/bit.

The super-regenerative technique is based on the startup of a harmonic oscillator [4]. Signal detection is achieved by sensing the variation of oscillation startup time. Startup time decreases with the strength of an external signal injected onto the oscillatory nodes, facilitating the detection of AM and OOK. However, without filtering frequency selectivity is poor. Therefore, a Q-enhanced (Q>1400) filter derived from an LC oscillator is used to suppress out-of-band signals. A periodic quench signal bias is used to make the oscillator first operate as a Q-enhanced filter, to suppress out-of-band signals, and then in the super-regenerative mode (i.e., enabling the oscillator) for detection. Receiver performance is directly determined by how well the active devices, in particular the bias current of the cross-coupled LC oscillator, are controlled. However, it is difficult to set the optimum quench signal on-chip for a fully integrated LC oscillator because of offsets as well as process and temperature variations. In order to implement a self-sustaining wireless node, an architecture that combines a DAC and a digital processor is proposed that runs the successive approximation register (SAR) algorithm, to control and automatically calibrate the receiver.

Figure 20.8.1 shows the system architecture of the proposed super-regenerative receiver. The incoming RF signal is first amplified by the LNA, whose input is matched to 50Ω at 2.4GHz, and then directly injected onto the oscillatory nodes of the VCO. Unlike other designs, the quench waveform is generated entirely on-chip by the 9b DAC quench generator. It supplies the bias current for the oscillator and controls the operating mode of the oscillator via the digital processor. The envelope detector senses oscillation and its outputs are fed to an offset-canceled preamplifier and comparator. The comparator output supplies digital demodulated data which streams into the digital processor. The integer-N frequency synthesizer tunes the frequency for narrow-band detection, enabling multi-channel (9 channels) communication.

The critical current I_{crit} is the value of oscillator bias current at which the active devices of the oscillator exactly compensate for the parasitic loss of the resonant tank. For an on-chip resonant tank, the exact value of this loss is difficult to determine; furthermore I_{crit} varies with temperature and operating frequency, resulting in inconsistent receiver selectivity and sensitivity. Since oscillation can only occur when the bias current is above I_{crit}, a SAR algorithm is used to search for the appropriate value of I_{crit}. As shown in Fig. 20.8.2, the 9b DAC quench generator first sets the bias current to midscale (i.e., MSB = 1) and reads the comparator output, checking for oscillation, to determine if this current value is larger than I_{crit}. The binary search continues to determine the full 9b bias current that is closest to, but below, I_{crit}. This value of I_{crit} results in the maximum enhanced Q. Once I_{crit} is known, the digital processor generates the corresponding quench control to maximize the selectivity and sensitivity.

Figure 20.8.3 shows the timing diagram and quench waveform. The receiver first tunes the tank frequency with the frequency synthesizer. Next, the system runs the SAR algorithm to determine I_{crit}. In detection mode, each detection period spans 10 clock cycles (5MHz). The receiver operates as a Q-enhanced filter for the first 4 cycles. It operates in super-regenerative mode, with exponentially growing bias, during the next 5 cycles for signal detection. Finally, the oscillator's bias current is turned off in the last cycle, quenching any oscillation. The comparator is enabled during the last 6 cycles and its output becomes logic 1, if and when, the VCO oscillates. The number of 1's in the data output, per detection period, accurately reflects the startup time. With a 5MHz clock, the quench frequency is 500kHz and the resulting data rate is 500kb/s. The measured turn-on time of the receiver is 83.6μs.

The prototype receiver is implemented in a 0.13μm mixed-mode CMOS process. The measured tuning range of the VCO is from 2.35 to 2.53GHz, which covers the entire ISM band, and the measured S_{11} is less than -12dB over the entire band (Fig. 20.8.1). The average number of 1's at the comparator output are measured versus input power, applying desired channel and adjacent channel (10MHz offset) signals. Figure 20.8.4(a) shows the measured sensitivity (min.=-90dBm) and the rejection of the adjacent channel signal. As shown in Fig. 20.8.4(b), with a 1.2V supply, signal rejection is -10dB at a 3MHz frequency offset. From this, the enhanced Q of the on-chip resonant circuit is calculated to be approximately 1400. The selectivity under different supply voltages is also measured and the result is shown in Fig. 20.8.4(b).

To test at higher data rates system clock is increased from 5MHz to 10MHz, corresponding to an increase in the quench frequency from 500kHz to 1MHz. As shown in Fig. 20.8.5(a), the minimum sensitivity increases from -90dBm to -60dBm, because of the reduced time for oscillation build-up. In addition, signal rejection is roughly halved since the time for Q-enhancement is also reduced. Figure 20.8.5(b) shows the BER measurements for 500kb/s pseudo-random NRZ data modulated on a 2.45GHz RF carrier. The measured BER is 0.1% for a -80dBm input and becomes 6.5% for a -90dBm input. The entire receiver, including the PLL, draws 2.4mA which corresponds to 5.6nJ per received bit at the data rate of 500kb/s. The measured receiver performance is summarized in Fig. 20.8.6 and the die micrograph is shown in Fig. 20.8.7.

Acknowledgements:
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References:

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[2] B. Otis et al., "A 400∝W-RX 1.6mW-TX Super-Regenerative Transceiver for Wireless Sensor Networks," *ISSCC Dig. Tech. Papers*, pp. 396–397, Feb., 2005.

[3] J.-Y. Chen, Michael P. Flynn, and John P. Hayes, "A 3.6mW 2.4-GHz Multi-Channel Super-Regenerative Receiver in 130nm CMOS," *Proc. IEEE CICC*, pp. 361-364, Sept., 2005.

[4] E. H. Armstrong, "Some Recent Developments of Regenerative Circuits," Proc. IRE, vol. 10, pp. 244-260, Aug., 1922.

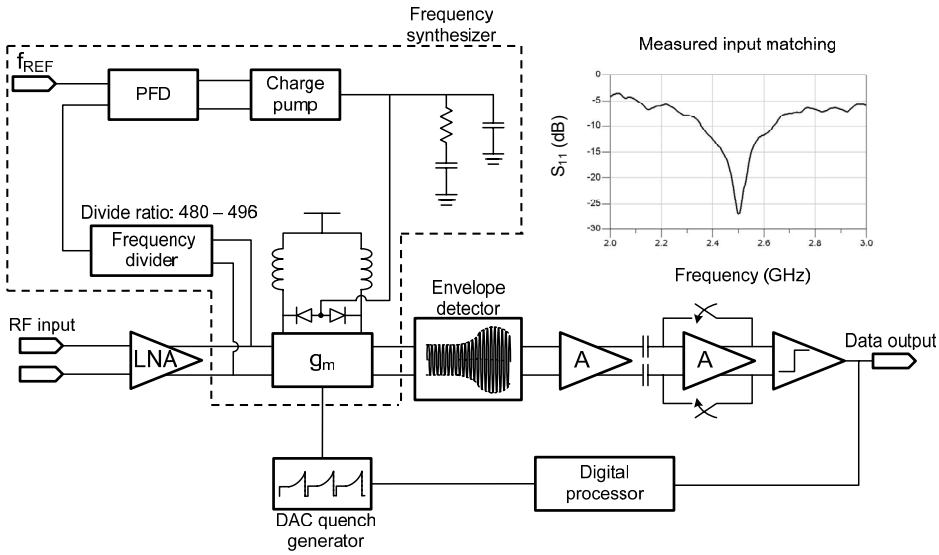

Figure 20.8.1: System architecture of the super-regenerative receiver.

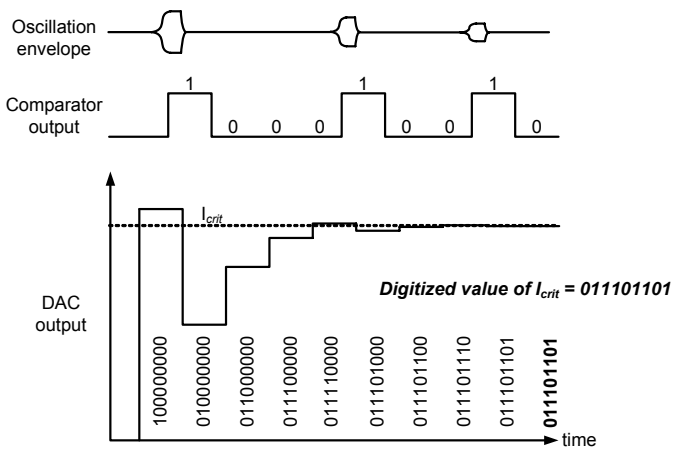

Figure 20.8.2: I_{crit} search with SAR algorithm.

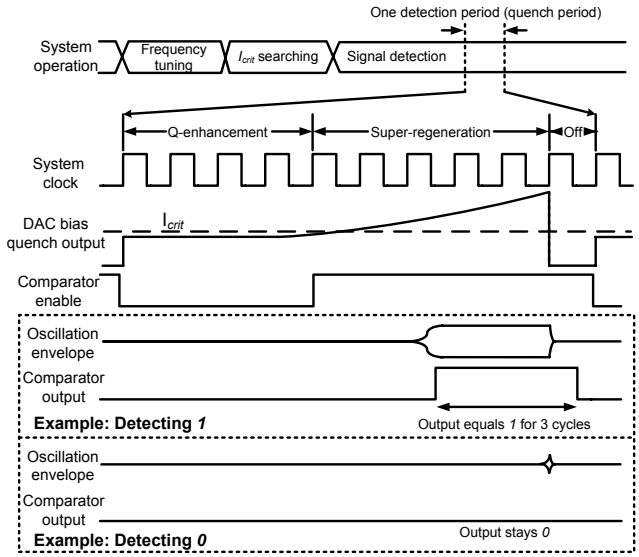

Figure 20.8.3: Timing diagram of the receiver operation.

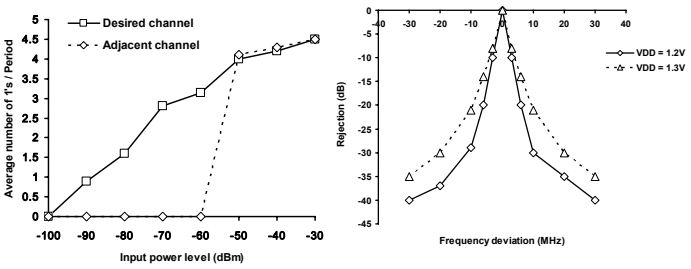

Figure 20.8.4: (a) Data output per period versus input power of desired and adjacent channel signals. (b) Signal rejection at 2.45GHz center frequency under different supply voltages.

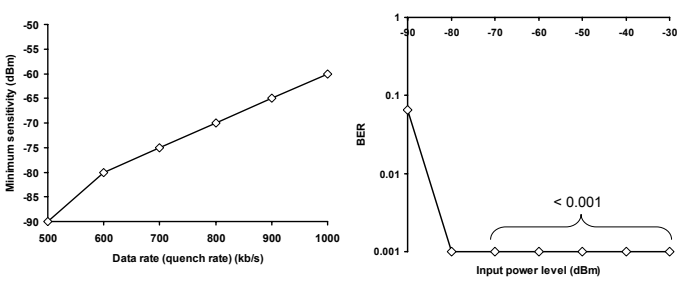

Figure 20.8.5: (a) Minimum sensitivity versus data rate for 2.45GHz center frequency. (b) BER versus input power level with a 500kHz quench signal (500kb/s PRBS signal) and 2.45GHz center frequency.

Continued on Page 660

Supply voltage	1.1 to 1.3V
Power consumption	2.8mW @ 1.2V
VCO tuning range	2.35 to 2.53GHz
Channel spacing	10MHz
Circuit area	1mm^2
Selectivity	900kHz @ –3dB (Q = 1400)
Sensitivity	–90dBm
Data rate	500kb/s @ 500kHz quench
	1Mb/s @ 1MHz quench (minimum sensitivity: –60dBm)
BER (≥ –80dBm input)	≤ 0.1%
Turn-on time	83.6µs
Energy per received bit	5.6nJ @ 500kHz quench
Technology	0.13µm CMOS

Figure 20.8.6: Summary of the measurement results.

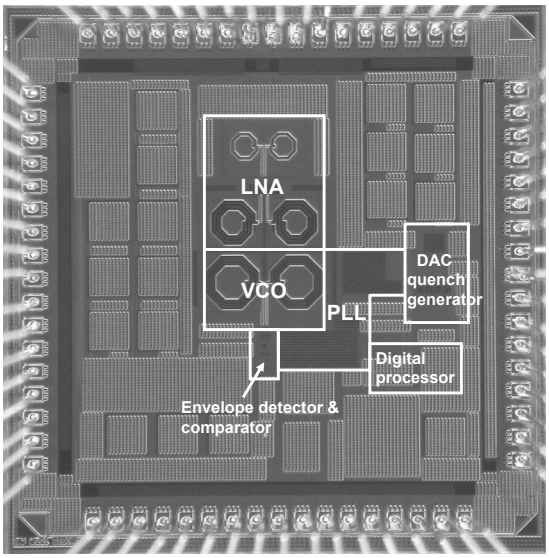

Figure 20.8.7: Die micrograph of the receiver.

